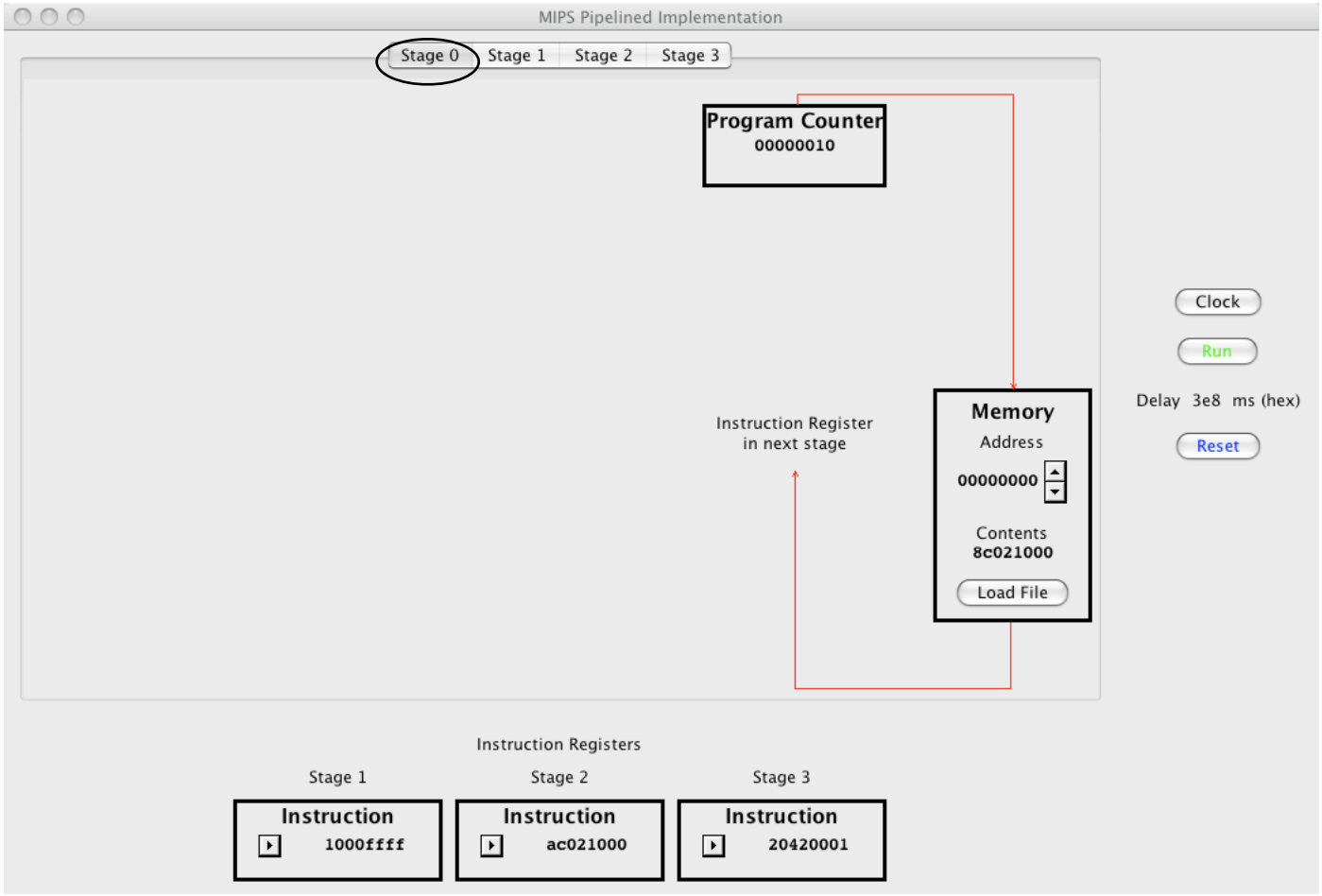
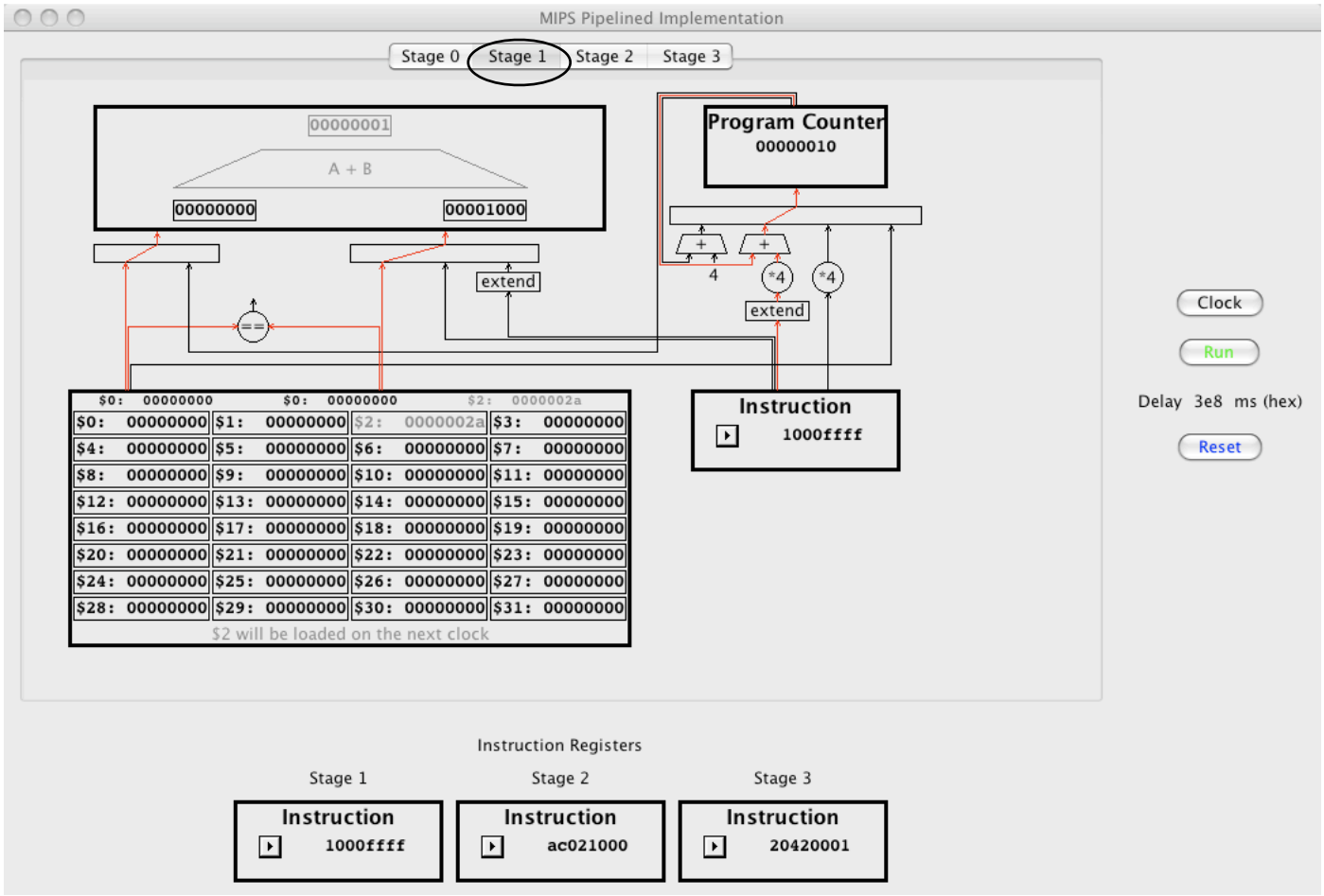
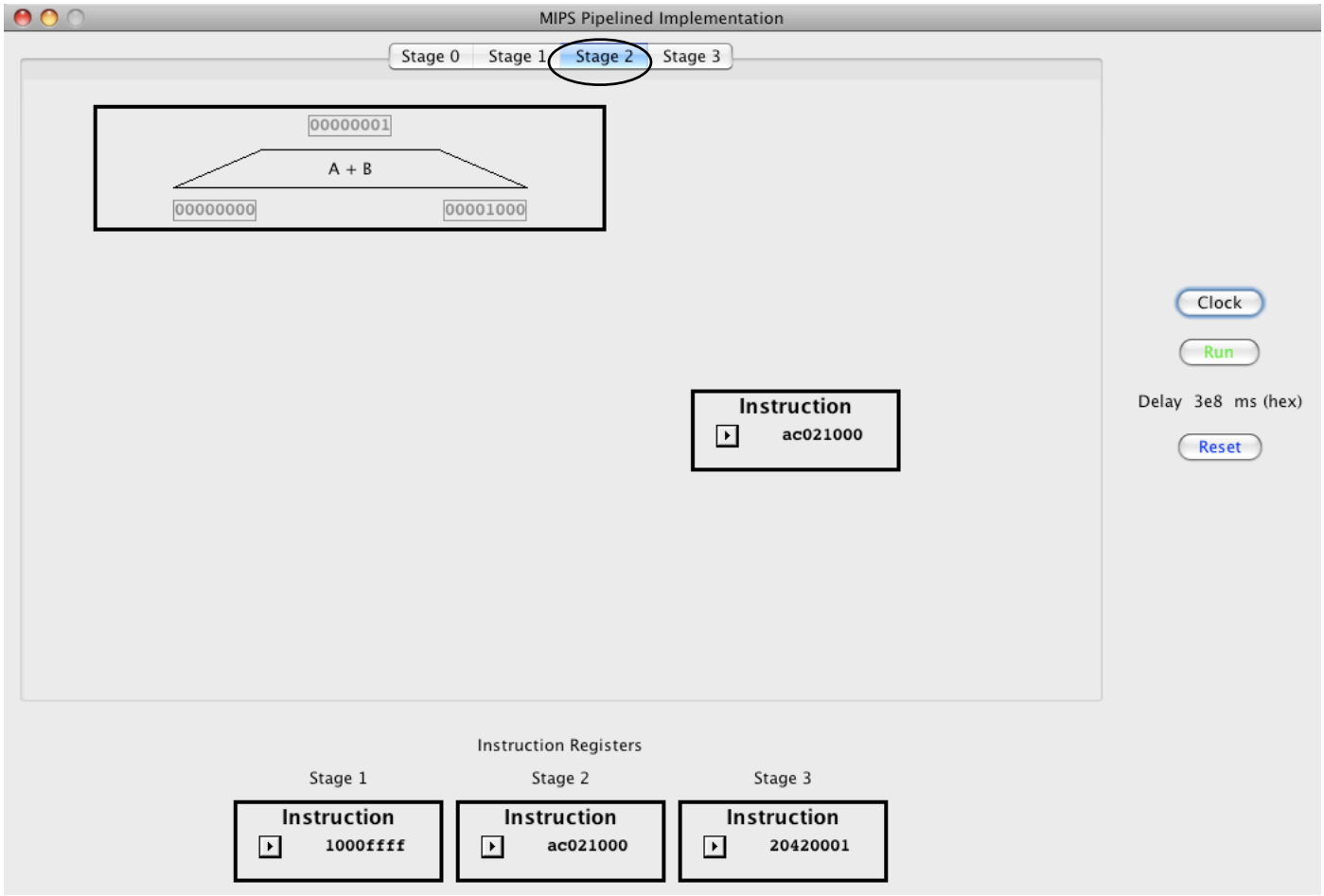
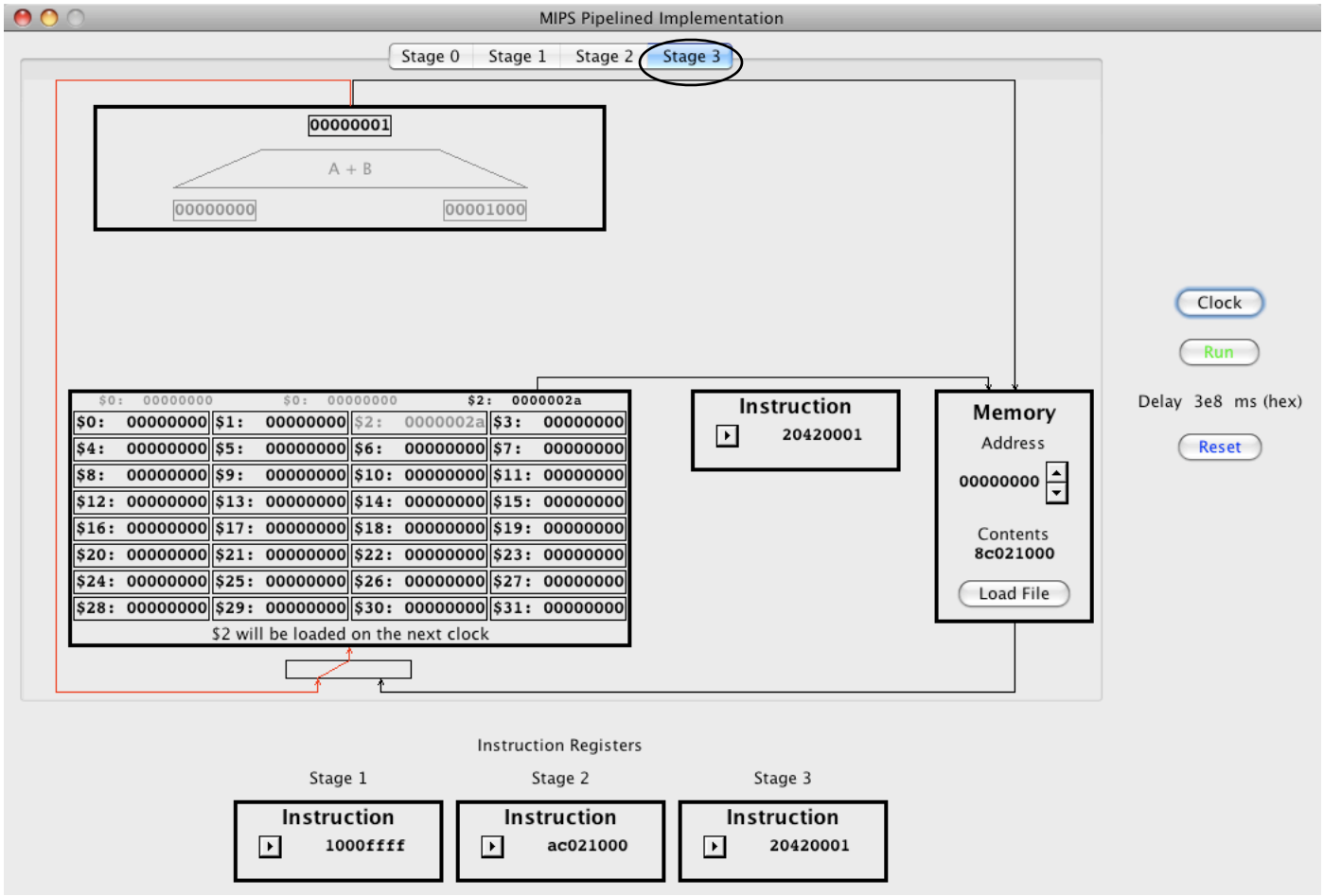
Stages in a Pipelined Implementation of the MIPS Architecture






MIPS Pipelined Implementation
Stage 0
Stage 1
Stage 2
Stage 3
00000001
A + B
00000000
00001000
Instruction
ac021000
Clock
Run
Delay 3e8 ms (hex)
Reset
Instruction Registers
Stage 1
Stage 2
Stage 3
Instruction
1000ffff
Instruction
ac021000
Instruction
20420001


MIPS Pipelined Implementation
Stage 0
Stage 1
Stage 2
Stage 3
00000001
A + B
00000000
00001000
$0: 00000000 $0: 00000000 $2: 0000002a
$0: 00000000 $1: 00000000 $2: 0000002a $3: 00000000
$4: 00000000 $5: 00000000 $6: 00000000 $7: 00000000
$8: 00000000 $9: 00000000 $10: 00000000 $11: 00000000
$12: 00000000 $13: 00000000 $14: 00000000 $15: 00000000
$16: 00000000 $17: 00000000 $18: 00000000 $19: 00000000
$20: 00000000 $21: 00000000 $22: 00000000 $23: 00000000
$24: 00000000 $25: 00000000 $26: 00000000 $27: 00000000
$28: 00000000 $29: 00000000 $30: 00000000 $31: 00000000
$2 will be loaded on the next clock
Instruction
20420001
Memory
Address
00000000
Contents
8c021000
Load File
Clock
Run
Delay 3e8 ms (hex)
Reset
Instruction Registers
Stage 1
Stage 2
Stage 3
Instruction
1000ffff
Instruction
ac021000
Instruction
20420001